Docket No.: 57454-011

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Akira YAMAZAKI, et al.

Serial No.: 09/780,477

Filed: February 12, 2001

Group Art Unit: 2816

Examiner: A. Q. TRA

For: MULTI-POWER SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

THE COMMISSIONER FOR PATENTS AND TRADEMARKS
Washington, DC 20231

Dear Sir:

Transmitted herewith is an Amendment in the above identified application.

☒ No additional fee is required.

☐ Applicant is entitled to small entity status under 37 CFR 1.27

☐ Also attached:

The fee has been calculated as shown below:

	NO. OF CLAIMS	HIGHEST PREVIOUSLY PAID FOR	EXTRA CLAIMS	RATE	FEE
Total Claims	20	20	0	$18.00 =	$0.00
Independent Claims	4	4	0	$84.00 =	$0.00
		Multiple claims newly presented			$0.00
		Fee for extension of time			$0.00
					$0.00
				Total of Above Calculations	$0.00

☐ Please charge my Deposit Account No. 500417 in the amount of $0.00. An additional copy of this transmittal sheet is submitted herewith.

☒ The Commissioner is hereby authorized to charge payment of any fees associated with this communication or credit any overpayment, to Deposit Account No. 500417, including any filing fees under 37 CFR 1.16 for presentation of extra claims and any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

MCDERMOTT, WILL & EMERY

David M. Tennant
Registration No. 48,362

600 13th Street, N.W.
Washington, DC 20005-3096
(202)756-8000 DT:men
Facsimile: (202)756-8087

Date: June 24, 2002

#5/Amdt A
6.27.02
C. Wills

PATENT

Docket No.: 57454-011

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of

Akira YAMAZAKI, et al.

Serial No.: 09/780,477 — Group Art Unit: 2816

Filed: February 12, 2001 — Examiner: A. Q. TRA

For: MULTI-POWER SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

AMENDMENT

Commissioner for Patents
Washington, DC 20231

Sir:

In response to the Office Action dated March 22, 2002, please amend this application as follows:

IN THE SPECIFICATION:

Page 13, first full paragraph now reads as follows:

A1

When the power supply voltage VDDL is applied or powered on at Tc, the power-on detection signal /PORL has its level once increased in response to the rising of the power supply voltage VDDL and then fixed at the "L" level. The output signal of the inverter 12b responsively attains the "H" level of the power supply voltage VDDL level to turn on the MOS transistor 12c. The node 12m is again reliably coupled to the ground node and held at the ground voltage level.